UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/682,579	10/08/2003	David T. Hass	RZMI-P101	8468

32986 7590 08/30/2005

IPSG, P.C.
P.O. BOX 700640
SAN JOSE, CA 95170-0640

EXAMINER	
THOMAS, SHANE M	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 08/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/682,579	HASS ET AL.	
	Examiner	Art Unit	
	Shane M. Thomas	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 October 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office action is responsive to the application filed 10/8/2003. Claims 1-32 are presented for examination.

The examiner requests, in response to this Office action, any reference(s) known to qualify as prior art under 35 U.S.C. sections 102 or 103 with respect to the invention as defined by the independent and dependent claims. That is, any prior art (including any products for sale) similar to the claimed invention that could reasonably be used in a 102 or 103 rejection. This **request** does not require applicant to perform a search. This request is not intended to interfere with or go beyond that **required** under 37 C.F.R. 1.56 or 1.105.

The request may be fulfilled by asking the attorney(s) of record handling prosecution and the inventor(s)/assignee for references qualifying as prior art. A simple statement that the query has been made and no prior art found is sufficient to fulfill the request. Otherwise, the fee and certification requirements of 37 CFR section 1.97 are waived for those documents submitted in reply to this request. This waiver extends only to those documents within the scope of this request that are included in the application's first complete communication responding to this requirement. Any supplemental replies subsequent to the first communication responding to this request and any information disclosures beyond the scope of this are subject to the fee and certification requirements of 37 CFR section 1.97.

In the event prior art documentation is submitted, a discussion of relevant passages, figs. etc. with respect to the claims is requested. The examiner is looking for specific references to 102/103 prior art that identify independent and dependent claim limitations. Since applicant is

most knowledgeable of the present invention and submitted art, his/her discussion of the reference(s) with respect to the instant claims is essential. **A response to this inquiry is greatly appreciated.**

The examiner also requests, in response to this Office action, that support be shown for language added to any original claims on amendment and any new claims. That is, indicate support for newly added claim language by specifically pointing to page(s) and line no(s). in the specification and/or drawing figure(s). This will assist the examiner in prosecuting the application.

Priority

Applicant's claim for domestic priority under 35 U.S.C. 119(e) is acknowledged for provisional applications 60/490,236, filed 7/25/2003, and 60/416,838, filed 10/8/2002. However, the provisional application 60/146,838 upon which priority is claimed fails to provide adequate support under 35 U.S.C. 112 for claims 2,4, and 5-32 of this application. The disclosure of 60/416,838 fails to disclose:

(1) [claim 2] the data switch interconnect coupled to each of the data caches of the processor cores;

(2) [claim 2] the messaging network coupled to the instruction cache of each of the processor cores;

(3) [claims 5-8] an interface switch interconnect coupled to the messaging network, a plurality of communication ports and configured to pass information between the network and ports;

(4) [claims 9-16] a memory bridge coupled to the data switch interconnect and at least one communications port and configured to communicate with the data switch interconnect and the communications port; and

(5) [claims 17-32] a super memory bridge coupled to the data switch interconnect, the interface switch interconnect, and at least one communications port and configured to communicate with the data switch interconnect, the interface switch interconnect, and the at least one communications port.

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: figure 1, element 10, and figure 2, element 100. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The disclosure is objected to because of the following informalities:

Regarding ¶24, the term --communication-- should be corrected to --communicate--.

Appropriate correction is required.

Claim Objections

Claims 1-32 are objected to because of the following informalities:

As per claims 1-32, the Examiner recommends amending all instances of the term --the processor cores-- with --the *multithreaded* processor cores-- as the term --processor cores-- were for coherency purposes. Appropriate correction is required.

Double Patenting

Claims 1, 2, 9, and 11, are directed to the same invention as that of claims 15-18 of commonly assigned application 10/930,179. The issue of priority under 35 U.S.C. 102(g) and possibly 35 U.S.C. 102(f) of this single invention must be resolved.

Since the U.S. Patent and Trademark Office normally will not institute an interference between applications or a patent and an application of common ownership (see MPEP § 2302), the assignee is required to state which entity is the prior inventor of the conflicting subject matter. A terminal disclaimer has no effect in this situation since the basis for refusing more than one patent is priority of invention under 35 U.S.C. 102(f) or (g) and not an extension of monopoly.

Failure to comply with this requirement will result in a holding of abandonment of this application.

A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

The scope of claims 1,2,9, and 11, of the present application are identical to the scope of claims 15-18 of the 10/930,179 application, respectively.

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-12, 25, and 27, are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-14 of copending Application No. 10/930,179. Although the conflicting claims are not identical, they are not patentably distinct from each other because the term --multithreaded processor core-- of present claim 1 is an obvious modification to the term --processor term-- of claim 1 of the 10/930,179 application. While application 10/930,179 does not explicitly claim a multithreaded processor core, the advantages of using a multithreaded processor core are well known in the art. Burkey et al. (U.S. Patent Application Publication No. 2004/0216120) teaches in ¶22 that a processor core capable of executing multiple threads increases system efficiency in that the core can switch threads while a particular thread is idle and waiting on other tasks to complete. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified the advanced processor of application 10/930,179 with the teaching of multithreaded processor cores of Burley in order to have increased the efficiency of the advanced processor system.

Thus, the scope of claims 1-12, 25, and 27 of the present application is an obvious modification to the scope of claims 1-14 of the 10/930,179 application.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claims 1-16 and 25-32 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-24 of copending Application No. 10/898,008 in view of *Computer Architecture: A Quantitative Approach* (herein Hennessy).

Although the conflicting claims are not identical, they are not patentably distinct from each other because the term --multithreaded processor core-- of present claim 1 is an obvious modification to the term --processor term-- of claims 1 of the 10/898,008 application. While application 10/898,008 does not explicitly claim a multithreaded processor core, the advantages of using a multithreaded processor core are well known in the art. Burkey et al. (U.S. Patent Application Publication No. 2004/0216120) teaches in ¶22 that a processor core capable of executing multiple threads increases system efficiency in that the core can switch threads while a particular thread is idle and waiting on other tasks to complete. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified the advanced processor of application 10/898,008 with the teaching of multithreaded processor cores of Burley in order to have increased the efficiency of the advanced processor system.

This is a provisional obviousness-type double patenting rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1 and 3 are rejected under 35 U.S.C. 102(e) as being anticipated by Joy et al. (U.S. Patent No. 6,694,347).

As per claim 1, Joy shows in figure 11 a plurality of multithreaded processor cores 1102,1104. Each core comprises a data cache and an instruction cache (not specifically shown in figure 11 - refer to figure 12, elements 1222 and 1212, respectively) - refer also to column 23, lines 15-42. A data switch interconnect 1125 is shown in figure 11 to be coupled to the cores 1102-1104 and configured to pass information from the L2 cache 1124 among the cores (column 23, lines 1-15). Finally, a messaging network is coupled to each of the processors by means of memory control unit 1128,1158 and a plurality if communication ports [ports that are contained on the DRAM modules 1134 that are used to access the DRAM].

As per claim 3, Joy shows in figure 11 an L2 cache 1124 that is coupled to the data switch interface 1125 and configured to store information accessible to the processor cores (column 23, lines 1-15).

Claims 1-32 are rejected under 35 U.S.C. 102(e) as being anticipated by Kohn et al. (U.S. Patent Application Publication No. 2003/0088610).

As per claim 1, Kohn shows an advanced processor in figure 5 that comprises a plurality of multi-threaded processor cores (118), each having a data cache and an instruction cache (¶28), a data switch interconnect 120 coupled to each of the cores (figure 3) and configured to transfer pass data among the processor cores from the L2 caches (figure 3 and ¶27). Figure 5 also shows a messaging network [control path which networks I/O devices 132 to the cores by way of the I/O bridge 134 and the data switch interconnect 120]. The Examiner is regarding the connections between the I/O bridge 134 and the I/O devices 132 to be --communication ports-- since the cores 118 can access data directly from any of the I/O devices (¶30).

As per claim 2, Kohn shows in figure 3 that the data switch interconnect 120 is coupled to each of the processor cores by means of each core's internal L1 cache. Since the L1 cache comprises both the instruction cache and the data cache (¶28), it can be seen that the data switch interconnect is coupled to the core by its respective data cache and its respective instruction cache. Therefore, lines 1-3 of claim 2 are anticipated. The messaging network, as defined *supra*, is connected to each of the cores through the I/O bridge 134 and the data switch interconnect 120 as discussed and as such, is coupled to the each of the processor cores by the data cache and the instruction cache, just as the data switch interconnect. Therefore, lines 4-5 of claim 2 is anticipated since the claims do not limit that the data switch interconnect and the messaging network being *directly* connected to the processor cores by the data or instruction cache and further since the limitations do not limit the data switch interconnect nor the messaging network to be coupled *only* to the data cache and instruction cache, respectively.

As per claims 3 and 4, Kohn shows in figure 5 a level two cache 122 coupled to the data interconnect switch 120. The level two caches are configured to store information accessible to the processor cores (¶27).

As per claims 5-8, Kohn shows an interface switch interconnect 130 coupled to the message network [i.e. the network between the I/O devices 132 though the I/O bridge 134] and the plurality of communication ports [by means of the I/O devices themselves]. The interface switch interconnect is configured to pass information among the messaging network and the communication ports (¶29).

As per claims 9-16, Kohn shows a memory bridge 126 in figure 5 as well. The memory bridge is coupled to the data switch interconnect by way of the L2 cache as shown and is further connected to a communications port (i.e. an inherent port on a corresponding one of the main memory modules of the system). The memory bridge 126 is configured to communicate with the data switch interconnect and the communications port to retrieve data from the system's main memory when requested by the processor core (¶28).

As per claims 17-32, Kohn shows a super memory bridge 134 coupled to the data switch interconnect 120, the interface switch interconnect 130 [by means of the I/O devices 132] and the communication ports that connect the I/O devices 132 to the super memory bridge. The super memory bridge 134 is configured to communicate with the data switch interconnected 120, the interface switch interconnect, and the communication port(s) as taught in ¶30.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Arimilli et al. (U.S. Patent No. 6,629,268) teaches an advanced processor in figures 1-2; however, the cores 30 only execute a single thread.

Barroso et al. (U.S. Patent Application Publication No. 2002/0046324) teaches an advanced processor in figure 1; however, Barroso does not specifically teach executing multiple threads on cores 110.

Kranich (U.S. Patent No. 6,574,725) teaches an advanced processor in figures 1-4 and utilizing synchronization logic 300 to execute multiple threads on processor cores 12A-12B.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane M Thomas whose telephone number is (571) 272-4188. The examiner can normally be reached M-F 8:30 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt M Kim can be reached at (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shane M. Thomas

HONG CHONG KIM
PRIMARY EXAMINER